# 4.2.13 Lane Margining at Receiver

Lane Margining at Receiver, as defined in this Section, is mandatory for all Ports supporting a data rate of 16.0 GT/s or higher, including Pseudo Ports (Retimers). Lane Margining at Receiver enables system software to obtain the margin information of a given Receiver while the Link is in the L0 state. The margin information includes both voltage and time, in either direction from the current Receiver position. For all Ports that implement Lane Margining at Receiver, Lane Margining at Receiver for timing is required, while support of Lane Margining at Receiver for voltage is optional at 16.0 GT/s and required at 32.0 GT/s and higher data rates. .

本节中定义的接收器链路余量测试对于所有支持16.0 GT/s或更高数据速率的端口（包括伪端口（Retimers））是强制性的。接收器处的链路余量使系统软件能够在链路处于L0状态时获得给定接收器的余量信息。余量信息包括从当前接收器位置沿任一方向的电压和时间。对于所有在接收器上实现链路余量测试的端口，需要在接收器上进行链路余量测试计时，而在16.0 GT/s和32.0 GT/s及更高的数据速率下，支持接收器上的链路余量测试电压是可选的。

Lane Margining at Receiver begins when a Margin Command is received, the Link is operating at 16.0 GT/s Data Rate or higher, and the Link is in L0 state. Lane Margining at Receiver ends when either a Go to Normal Settings command is received, the Link changes speed, or the Link exits either the L0 or Recovery states. Lane Margining at Receiver optionally ends when certain error thresholds are exceeded. Lane Margining at Receiver is is permitted to be suspended while the Link is in Recovery for independent samplers.

当接收到余量测试命令，链路以16.0 GT/s或更高的数据速率运行，并且链路处于L0状态时，接收器处的链路余量测试开始。当接收到“转到正常设置”命令、链路更改速度或链路退出L0或恢复状态时，接收器处的链路余量测试结束。当超过某些错误阈值时，接收器处的链路余量测试可选择结束。当链路处于独立采样器的恢复状态时，允许暂停接收器处的链路余量测试。

Lane Margining at Receiver is not supported by PCIe Links operating at 2.5 GT/s, 5.0 GT/s, or 8.0 GT/s.

Software uses the per-Lane Margining Lane Control Register and Margining Lane Status Register in each Port (Downstream or Upstream) for sending Margin Commands and obtaining margin status information for the corresponding Receiver associated with the Port. For the Retimers, the commands to get information about the Receiver's capabilities and status and the commands to margin the Receiver are conveyed in the Control SKP Ordered Sets in the Downstream direction. The status and error reporting of the target Retimer Receiver is conveyed in the Control SKP Ordered Sets in the Upstream direction. Software controls margining in the Receiver of a Retimer by writing to the appropriate bits in the Margining Lane Control Register in the Downstream Port. The Downstream Port also updates the status information conveyed by the Retimer(s) in the Link through the Control SKP Ordered Set into its Margining Lane Status Register.

以2.5 GT/s、5.0 GT/s或8.0 GT/s运行的PCIe链路不支持接收器处的链路余量测试。

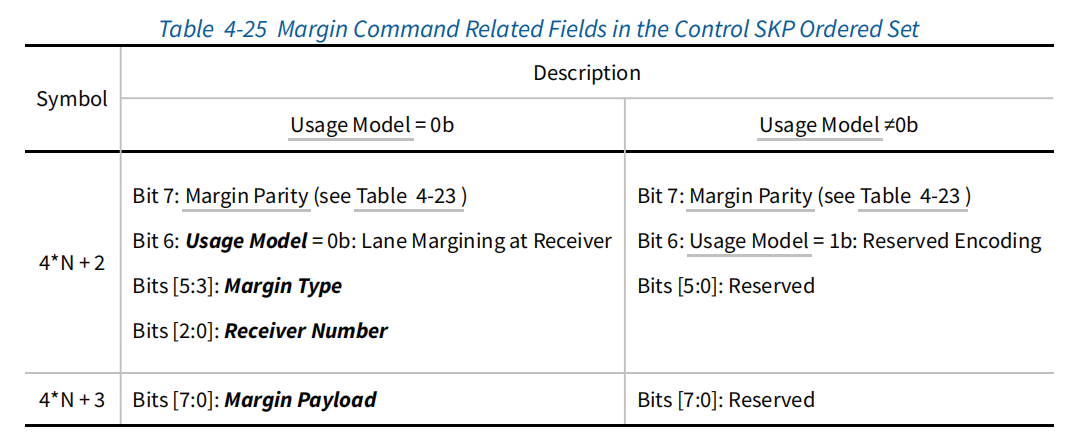
软件使用每个端口（下游或上游）中的每个通道链路余量测试控制寄存器和链路余量测试状态寄存器发送余量命令，并获取与该端口相关的相应接收器的余量状态信息。对于Retimer，获取接收器能力和状态信息的命令以及余量接收器的命令在下游方向的控制SKP有序集中传送。目标Retimer接收器的状态和错误报告在上游方向的控制SKP有序集合中传送。软件通过写入下游端口的链路余量测试控制寄存器中的适当位来控制Retimer接收器中的余量。下游端口还更新链路中Retimer通过控制SKP有序集传递到其链路余量测试状态寄存器中的状态信息。

## 4.2.13.1 Receiver Number, Margin Type, Usage Model, and Margin Payload Fields

The contents of the four command fields of the Margining Lane Control Register in the Downstream Port are always reflected in the identical fields in the Downstream Control SKP Ordered Sets. The contents of the Upstream Control SKP Ordered Set received in the Downstream Port is always reflected in the corresponding status fields of the Margining Lane Status Register in the Downstream Port. The following table provides the bit placement of these fields in the Control SKP Ordered Set.

4.2.13.1接收器编号、裕量类型、使用模型和裕量有效载荷字段

下游端口中的链路余量测试控制寄存器的四个命令字段的内容总是反映在下游控制SKP有序集中的相同字段中。在下游端口中接收的上游控制SKP有序集的内容总是反映在下游端口的链路余量测试状态寄存器的相应状态字段中。下表提供了这些字段在控制SKP顺序集中的位位置。



Usage Model: An encoding of 0b indicates that the usage model is Lane Margining at Receiver. An encoding of 1b in this field is reserved for future usages.

If the Usage Model field is 1b, Bits [5:0] of Symbol 4N+2 and Bits [7:0] of Symbol 4N+3 are Reserved.

When evaluating received Control SKP Ordered Set for Margin Commands, all Receivers that do not comprehend the usage associated with Usage Model = 1b are required to ignore Bits[5:0] of Symbol 4N+2 and Bits[7:0] of Symbol 4N+3 of the Control SKP Ordered Set, if the Usage Model field is 1b.

使用模型：0b的编码表示使用模型是接收器处的链路余量。在该字段中保留1b的编码以供将来使用。

如果使用模型字段是1b，则保留符号4N+2的位[5:0]和符号4N+3的位[7:0]。

当针对余量命令评估所接收的控制SKP有序集时，如果使用模型字段为1b，则不理解与使用模型＝1b相关联的使用的所有接收器被要求忽略控制SKP顺序集的符号4N+2的位[5:0]和符号4N+3的位[7:0]。

**IMPLEMENTATION NOTE**

Potential future usage of Control SKP Ordered Set

The intended usage for the 15 bits of information in the Control SKP Ordered Set, as defined in Table 4-25 is Lane Margining at Receiver. However a single bit (Bit 7 of Symbol 4N+2) is Reserved for any future usage beyond Lane Margining at Receiver. If such a usage is defined in the future, this bit will be set to 1b and the remaining 14 bits can be defined as needed by the new usage model. Alternatively, Symbol 4N could use a different encoding than 78h for any future usage, permitting all bits in Symbols 4N+1, 4N+2, and 4N+3 to be defined for that usage model.

实施说明

Control SKP有序集的潜在未来用途

如表4-25中所定义的，控制SKP有序集合中15位信息的预期用途是接收器处的链路余量。然而，单个比特（符号4N+2的比特7）被保留用于接收器处的链路余量之外的任何未来用途。如果将来定义这样的使用，则该比特将被设置为1b，并且剩余的14比特可以根据新的使用模型的需要来定义。或者，符号4N可以使用与78h不同的编码用于任何未来的使用，从而允许为该使用模型定义符号4N+1、4N+2和4N+3中的所有比特。

Receiver Number: Receivers are identified in Figure 4-35 . The following Receiver Number encodings are used in the Downstream Port for Margin Commands targeting that Downstream Port or a Retimer below that Downstream Port:

接收器编号：接收器如图4-35所示。以下接收器编号编码用于针对该下游端口或该下游端口下方的重定时器的余量命令的下游端口：

**000b**

Broadcast (Downstream Port Receiver and all Retimer Pseudo Port Receivers)

**001b**

Rx(A) (Downstream Port Receiver)

**010b**

Rx(B) (Retimer X or Z Upstream Pseudo Port Receiver)

**011b**

Rx(C) (Retimer X or Z Downstream Pseudo Port Receiver)

**100b**

Rx(D) (Retimer Y Upstream Pseudo Port Receiver)

**101b**

Rx(E) (Retimer Y Downstream Pseudo Port Receiver)

**110b**

Reserved

**111b**

Reserved

The following Receiver Number encodings are used in the Upstream Port for Margin Commands targeting that Upstream Port:

以下接收器编号编码用于针对该上游端口的余量命令的上游端口：

**000b**

Broadcast (Upstream Port Receiver)

**001b**

Reserved

**010b**

Reserved

**011b**

Reserved

**100b**

Reserved

**101b**

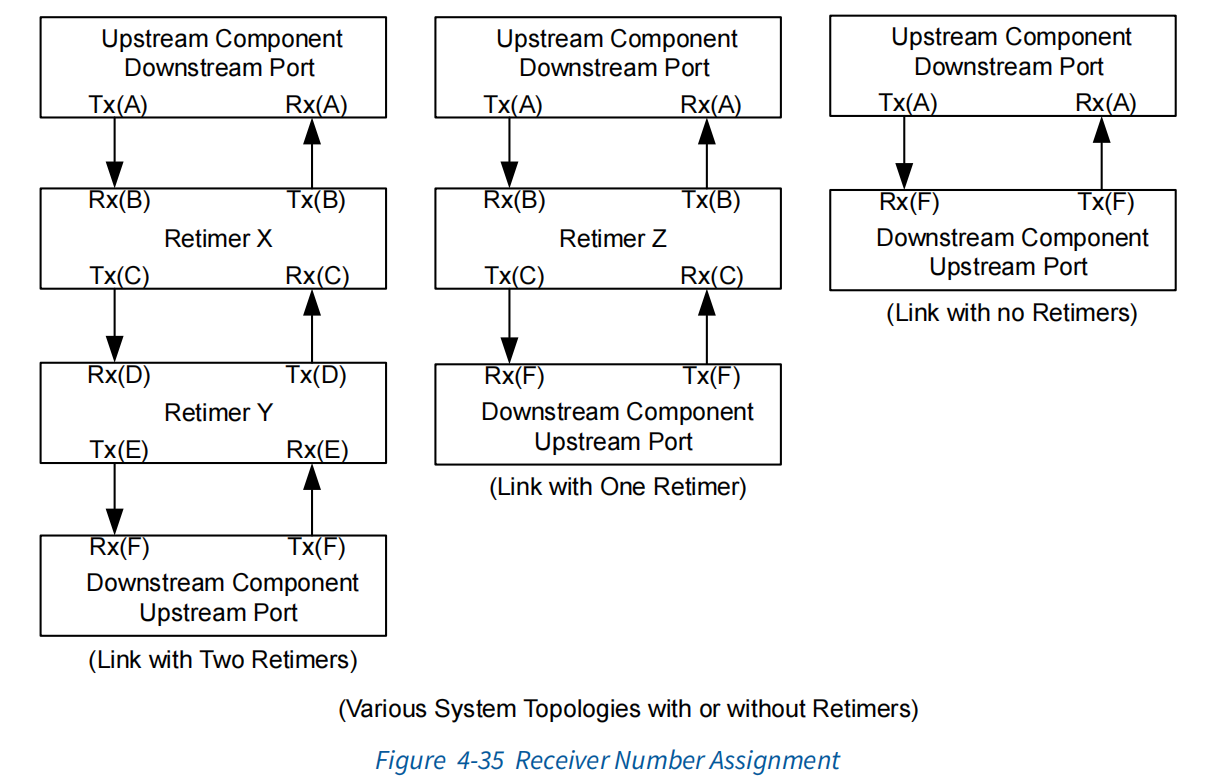
Reserved

**110b**

Rx (F) (Upstream Port Receiver)

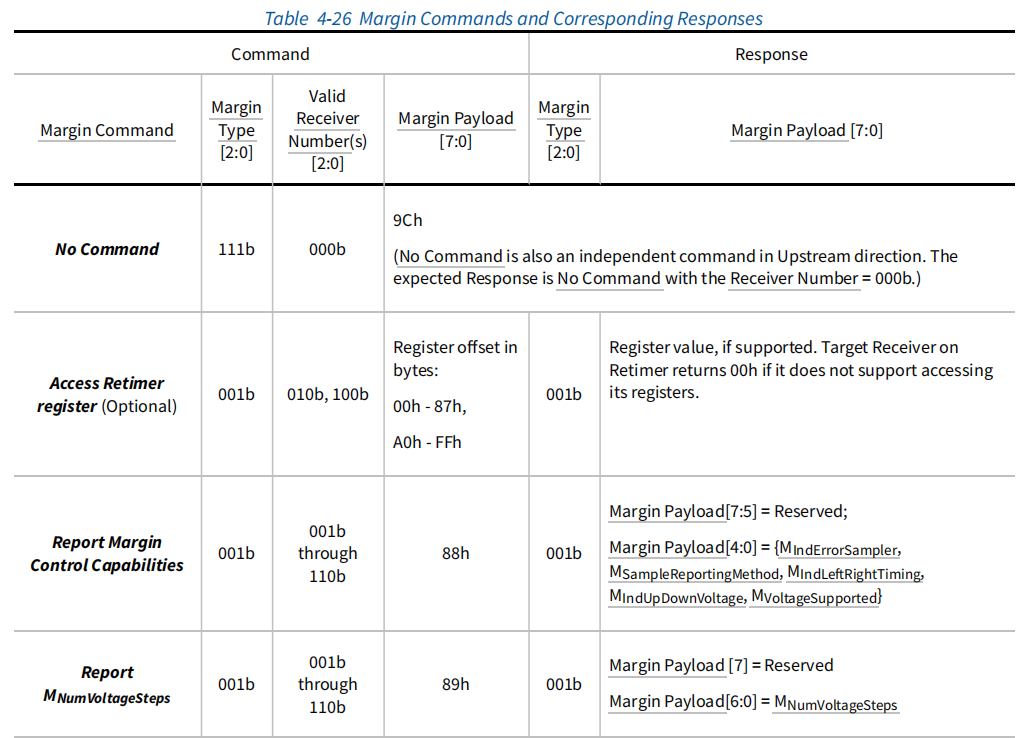
**111b**

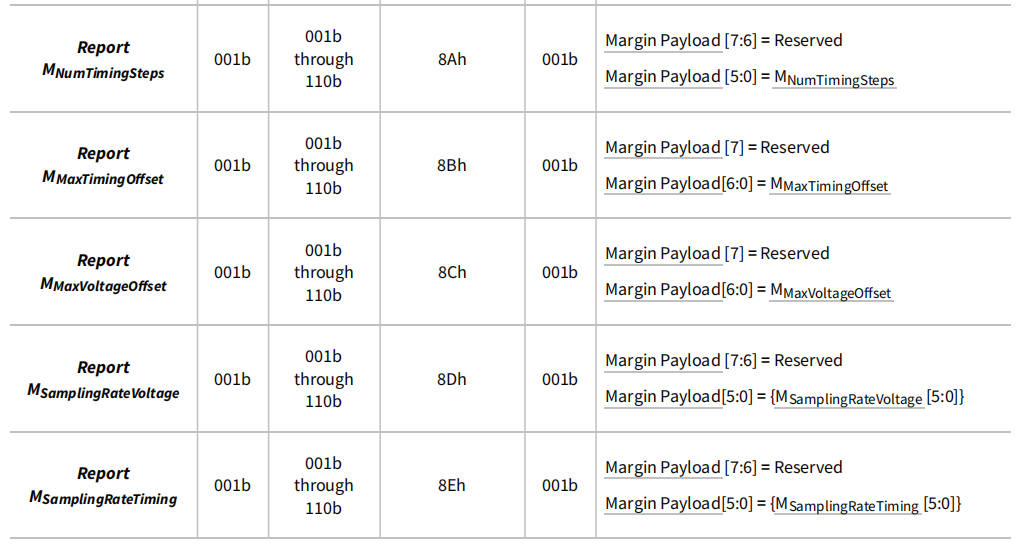
Reserved

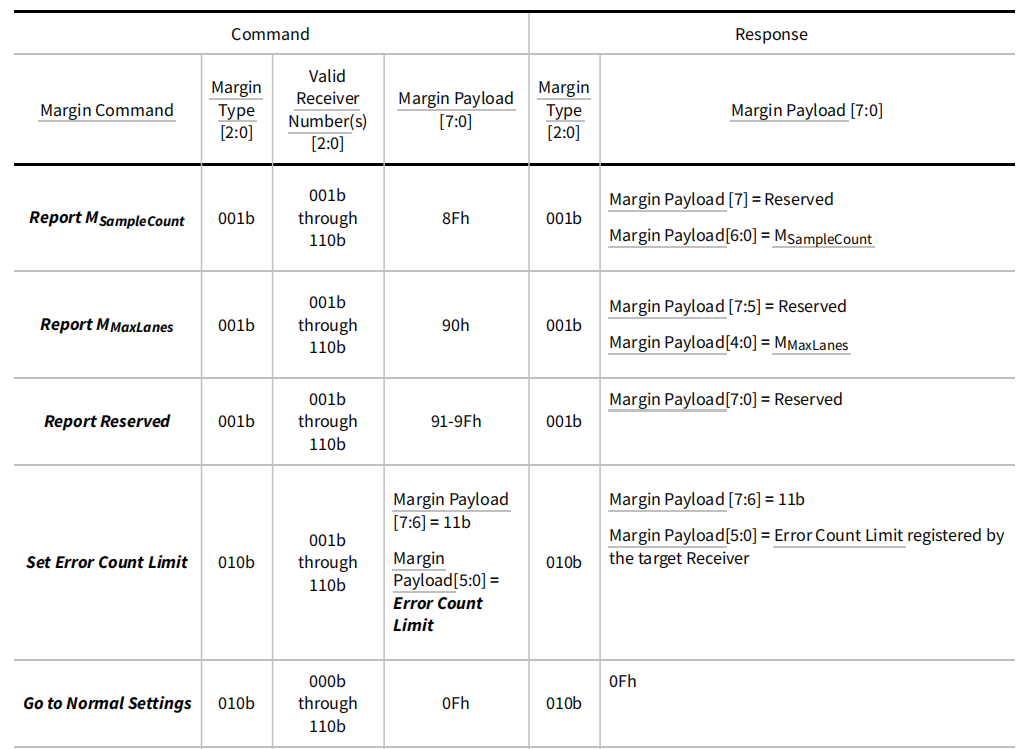


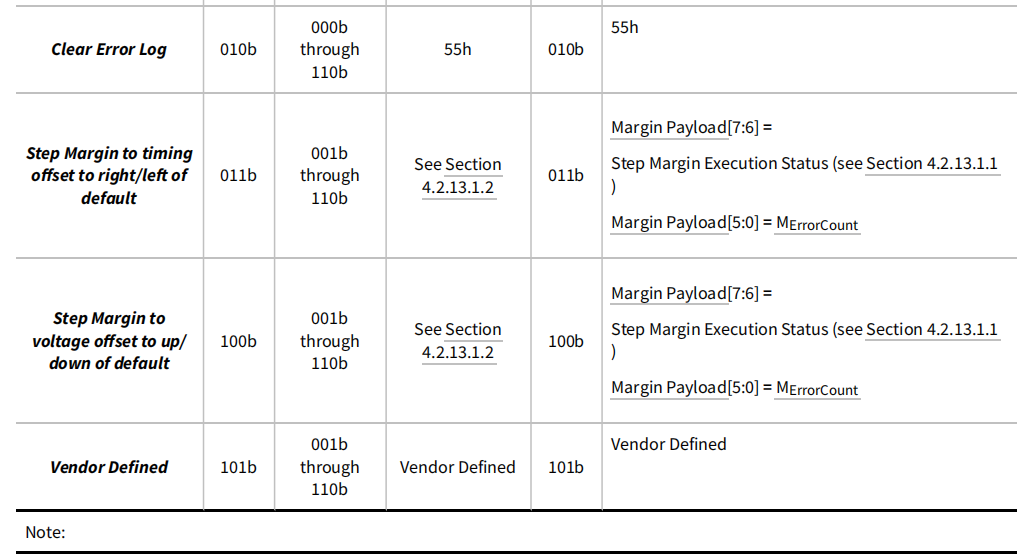
Margin Type and Margin Payload: The Margin Type field together with a valid Receiver Number(s), associated with the Margin Type encoding, and specific Margin Payload field define various commands used for margining (referred to as ***Margin Command***). Table 4-26 defines the encodings of valid Margin Commands along with the corresponding responses, used in both the Control SKP Ordered Sets as well as the Margining Lane Control Register and Margining Lane Status Register. Margin commands that are always broadcast will use the broadcast encoding for the Receiver Number, even when only one Receiver is the target (e.g., UP or a DP in a Link with no Retimers). The Receiver Number field in the response to a Margin Command other than No Command reflects the number of the Receiver that is responding, even for a Margin Command that is broadcast. The Margin Commands go Downstream whereas the responses go Upstream in the Control SKP Ordered Sets. The responses reflect the Margin Type to which the target Receiver is responding. The Receiver Number field of the response corresponds to the target Receiver that is responding. The various parameters such as MSampleCount used here are defined in Section 8.4.4 . All the unused encodings described below are Reserved and must not considered to be a valid Margin Command.

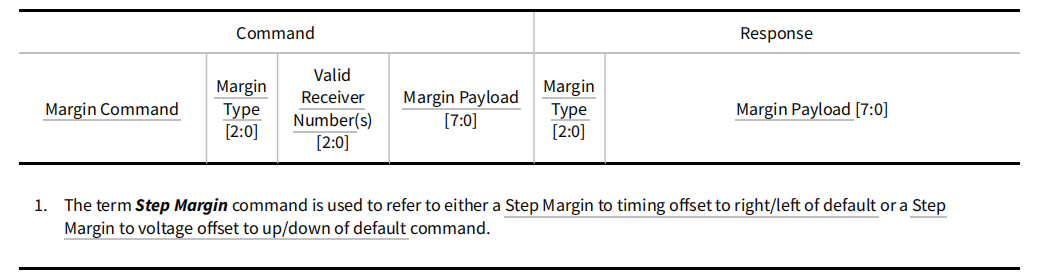
余量类型和余量有效载荷：余量类型字段以及与余量类型编码相关的有效接收器编号和特定的余量有效载荷字段定义了用于余量测试的各种命令（称为余量命令）。表4-26定义了有效余量命令的编码以及相应的响应，用于控制SKP有序集以及链路余量测试控制寄存器和链路余量测试状态寄存器。始终广播的余量命令将使用接收器编号的广播编码，即使只有一个接收器是目标（例如，没有Retimers的链路中的UP或DP）。对除“无命令”以外的余量命令的响应中的“接收器编号”字段反映了正在响应的接收器的编号，即使对于广播的余量指令也是如此。在控制SKP有序集合中，余量命令进入下游，而响应进入上游。响应反映了目标接收器正在响应的余量类型。响应的Receiver Number字段对应于正在响应的目标Receiver。第8.4.4节中定义了此处使用的各种参数，如MSampleCount。下面描述的所有未使用的编码都是保留的，不得视为有效的余量命令。











### 4.2.13.1.1 Step Margin Execution Status

The ***Step Margin Execution Status*** used in Table 4-26 is a 2-bit field defined as follows:

**11b**

NAK. Indicates that an unsupported Lane Margining command was issued. For example,timing margin beyond ±0.2 UI. MErrorCount is 0.

**10b**

Margining in progress. The Receiver is executing a Step Margin command. MErrorCount reflects the number of errors detected as defined in Section 8.4.4 .

4.2.13.1.1阶跃余量执行状态

表4-26中使用的阶跃余量执行状态是一个2位字段，定义如下：

11b

NAK。表示发出了不受支持的链路余量测试命令。例如，定时余量超过±0.2 UI。错误计数为0。

10b

正在进行余量测试。接收器正在执行步长余量命令。MErrorCount反映了第8.4.4节中定义的检测到的错误数量。

**01b**

Set up for margin in progress. This indicates the Receiver is getting ready but has not yet started executing a Step Margin command. MErrorCount is 0.

**00b**

Too many errors - Receiver autonomously went back to its default settings. MErrorCount reflects the number of errors detected as defined in Section 8.4.4 . Note that MErrorCount might be greater than Error Count Limit.

01b

正在设置余量。这表示接收器正在准备就绪，但尚未开始执行步长余量命令。错误计数为0。

00b

错误太多-接收器自动返回到其默认设置。MErrorCount反映了第8.4.4节中定义的检测到的错误数量。请注意，MErrorCount可能大于Error Count Limit。

### 4.2.13.1.2 Margin Payload for Step Margin Commands

For the Step Margin to timing offset to right/left of default command, the Margin Payload field is defined as follows:

• Margin Payload [7]: Reserved.

• If MIndLeftRightTiming for the targeted Receiver is Set:

◦ Margin Payload [6] indicates whether the Margin Command is right vs left. A 0b indicates to move the Receiver to the right of the normal setting whereas a 1b indicates to move the Receiver to the left of the normal setting.

◦ Margin Payload [5:0] indicates the number of steps to the left or right of the normal setting.

4.2.13.1.2阶跃余量命令的余量有效载荷

对于默认命令的向右/向左的步进余量到定时偏移，余量有效载荷字段定义如下：

•余量有效载荷[7]：保留。

•如果设置了目标接收器的MIndLeftRightTiming：

◦ 余量有效载荷[6]指示余量命令是向右还是向左。0b表示将接收器移至正常设置的右侧，而1b表示将接收器移到正常设置的左侧。

◦ 余量有效载荷[5:0]表示正常设置左侧或右侧的步数。

• If MIndLeftRightTiming for the targeted Receiver is Clear:

◦ Margin Payload [6]: Reserved

◦ Margin Payload [5:0] indicates the number of steps beyond the normal setting.

For the Step Margin to voltage offset to up/down of default command, the Margin Payload field is defined as follows:

•如果目标接收器的MIndLeftRightTiming为Clear（清除）：

◦ 余量有效载荷[6]：保留

◦ 余量有效载荷[5:0]表示超出正常设置的步数。

对于向上/向下默认命令的阶跃余量到电压偏移，余量有效载荷字段定义如下：

• If MIndUpDownVoltage for the targeted Receiver is Set:

◦ Margin Payload [7] indicates whether the Margin Command is up vs down. A 0b indicates to move the Receiver up from the normal setting whereas a 1b indicates to move the Receiver down from the normal setting.

◦ Margin Payload [6:0] indicates the number of steps up or down from the normal setting.

• If MIndUpDownVoltage for the targeted Receiver is Clear:

◦ Margin Payload [7]: Reserved

◦ Margin Payload [6:0] indicates the number of steps beyond the normal setting.

•如果设置了目标接收器的MIndUpDownVoltage：

◦ 余量有效载荷[7]指示余量命令是向上还是向下。0b表示从正常设置向上移动接收器，而1b表示从正常设定向下移动接收器。

◦ 余量有效载荷[6:0]表示从正常设置向上或向下的步数。

•如果目标接收器的MIndUpDownVoltage为Clear（清除）：

◦ 余量有效载荷[7]：保留

◦ 余量有效载荷[6:0]表示超出正常设置的步数。

## 4.2.13.2 Margin Command and Response Flow

Each Receiver advertises its capabilities as defined in Section 8.4.4 . The Receiver being margined must report the number of errors that are consistent with data samples occurring at the indicated location for margining. For simplicity, the Margin Commands and requirements are described in terms of moving the data sampler location though the actual margining method may be implementation specific. For example, the timing margin could be implemented on the actual data sampler or an independent/error sampler. Further, the timing margin can be implemented by injecting an appropriate amount of stress/jitter to the data sample location, or by actually moving the data/error sample location.

4.2.13.2余量指令和响应流程

每个接收方宣传其在第8.4.4节中定义的能力。被余量化的接收方必须报告与指定余量化位置发生的数据样本一致的错误数量。为了简单起见，余量命令和要求是根据移动数据采样器位置来描述的，尽管实际的余量方法可能是特定于实现的。例如，时序余量可以在实际数据采样器或独立/误差采样器上实现。此外，可以通过向数据采样位置注入适当量的应力/抖动，或者通过实际移动数据/误差采样位置来实现时序余量。

When an independent data/error sampler is used, the errors encountered with the independent data/error sampler must be reported in MErrorCount even though the Link may not experience any errors. To margin a Receiver, Software moves the target Receiver to a voltage/timing offset from its default sampling position.

The following rules must be followed:

当使用独立的数据/错误采样器时，即使链路可能没有出现任何错误，也必须在MErrorCount中报告独立数据/错误取样器遇到的错误。为了使接收器余量，软件将目标接收器移动到其默认采样位置的电压/定时偏移处。

必须遵守以下规则：

• Every Retimer Upstream Pseudo Port Receiver and the Downstream Port Receiver must compute the Margin CRC and Margin Parity bits and compare against the received Margin CRC and Margin Parity bits. Any mismatch must result in ignoring the contents of Symbols 4N+2 and 4N+3. A Downstream Port Receiver must report Margin CRC and Margin Parity errors in the Lane Error Status Register (see Section 7.7.3.3 ).

• The Upstream Port Receiver is permitted to ignore the Margin CRC bits, Margin Parity bits, and all bits in the Symbols 4N+2 and 4N+3 of the Control SKP Ordered Set. If it checks Margin CRC and Margin Parity, any mismatch must be reported in the Lane Error Status Register.

•每个Retimer上游伪端口接收器和下游端口接收器必须计算余量CRC和余量奇偶校验位，并与接收到的裕量CRC和裕量奇偶校验位进行比较。任何不匹配都必须导致忽略符号4N+2和4N+3的内容。下行端口接收器必须在通道错误状态寄存器中报告余量CRC和余量奇偶校验错误（见第7.7.3.3节）。

•允许上行端口接收器忽略余量CRC位、余量奇偶校验位以及控制SKP有序集的符号4N+2和4N+3中的所有位。如果检查了余量CRC和余量奇偶校验，则必须在通道错误状态寄存器中报告任何不匹配。

• The Downstream Port must transmit Control SKP Ordered Sets in each Lane, with the Margin Type, Receiver Number, Usage Model, and Margin Payload fields reflecting the corresponding control fields in the Margining Lane Control Register. Any Control SKP Ordered Set transmitted more than 10 μs after the Configuration Write Completion must reflect the Margining Lane Control Register values written by that Configuration Write.

◦ This requirement applies regardless of the values in the Margining Lane Control Register.

◦ This requirement applies regardless of the number of Retimer(s) in the Link.

•下游端口必须在每个通道中传输控制SKP有序集，余量类型、接收器编号、使用型号和余量有效载荷字段反映链路余量测试控制寄存器中的相应控制字段。配置写入完成后超过10μs传输的任何控制SKP有序集必须反映该配置写入写入的链路余量测试控制寄存器值。

◦ 无论链路余量测试控制寄存器中的值如何，此要求均适用。

◦ 无论链接中Retimer的数量如何，此要求都适用。

• For Control SKP Ordered Sets received by the Upstream Pseudo Port, a Retimer Receiver is the target of a valid Margin Command, if all of the following conditions are true:

◦ the Margin Type is not No Command

◦ the Receiver Number is the number assigned to the Receiver, or Margin Type is either Clear Error Log or Go to Normal Settings and the Receiver Number is 'Broadcast'.

◦ the Usage Model field is 0b

◦ the Margin Type, Receiver Number, and Margin Payload fields are consistent with the definitions in Table 4-25 and Table 4-26

◦ the Margin CRC check and Margin Parity check pass.

•对于上游伪端口接收到的控制SKP有序集，如果以下所有条件都成立，则重定时器接收器是有效余量命令的目标：

◦ 余量类型不是“无命令”

◦ 接收器编号是分配给接收器的编号，或者余量类型是清除错误日志或转到正常设置，并且接收器编号是“广播”。

◦ “使用模型”字段为0b

◦ 余量类型、接收器编号和余量有效载荷字段与表4-25和表4-26中的定义一致

◦ Margin CRC校验和Margin奇偶校验通过。

• For Upstream and Downstream Ports, a Receiver is the target of a valid Margin Command, if all of the following conditions are true for its Margining Lane Control Register:

◦ the Margin Type is not No Command

◦ the Receiver Number is the number assigned to the Receiver or Margin Type is either Clear Error Log or Go to Normal Settings and the Receiver Number is 'Broadcast'

◦ the Usage Model field is 0b

◦ the Margin Type, the Receiver Number, and Margin Payload fields are consistent with the definitions in Table 4-26

•对于上游和下游端口，如果其链路余量测试控制寄存器满足以下所有条件，则接收器是有效余量命令的目标：

◦ 余量类型不是“无命令”

◦ 接收器编号是分配给接收器的编号，或者余量类型是清除错误日志或转到正常设置，并且接收器编号是“广播”

◦ “使用模型”字段为0b

◦ 余量类型、接收器编号和余量有效载荷字段与表4-26中的定义一致

• The Upstream Port must transmit the Control SKP Ordered Set with No Command.

• A target Receiver must apply and respond to the Margin Command within 1ms of receiving the valid Margin Command if the Link is still in L0 state and operating at 16.0 GT/s or higher Data Rate.

◦ A target Receiver in a Retimer must send a response in the Control SKP Ordered Set in the Upstream Direction within 1 ms of receiving the Margin Command.

•上行端口必须在无命令的情况下传输控制SKP有序集。

•如果链路仍处于L0状态并以16.0 GT/s或更高的数据速率运行，目标接收器必须在收到有效余量命令后1ms内应用并响应余量命令。

◦ Retimer中的目标接收器必须在接收到余量命令的1ms内，在上游方向上的控制SKP有序集合中发送响应。

◦ A target Receiver in the Upstream Port must update the Status field of the Lane Margin Command and Status register within 1 ms of receiving the Margin Command.

◦ A target Receiver in the Downstream Port must update the Status field of the Lane Margin Command and Status register within 1 ms of receiving the Margin Command if the command is not broadcast or no Retimer(s) are present

◦ 上游端口中的目标接收器必须在接收到余量命令后1毫秒内更新链路余量命令和状态寄存器的状态字段。

◦ 下游端口中的目标接收器必须在接收到余量命令后1 ms内更新链路余量命令和状态寄存器的状态字段（如果该命令未广播或不存在Retimer）

• For a valid Margin Type, other than No Command, that is broadcast and received by a Retimer:

◦ A Retimer, in position X (see Figure 4-35 ), forwards the response unmodified in the Upstream Control SKP Ordered Set, if the command has been applied, else it sends the No Command.

◦ The Receiver Number field of the response must be set to an encoding of one of the Retimer's Pseudo Ports.

◦ The Retimer must respond only after both Pseudo Ports have completed the Margin Command.

•对于Retimer广播和接收的有效余量类型（无命令除外）：

◦ 位于位置X（见图4-35）的Retimer在上游控制SKP有序集合中转发未修改的响应，如果已应用命令，则发送“无命令”。

◦ 响应的Receiver Number字段必须设置为Retimer的伪端口之一的编码。

◦ 只有在两个伪端口都完成了余量命令后，Retimer才能做出响应。

• The Retimer must overwrite Bits [4:0] of Symbol 4N+1, Bits[7, 5:0] of Symbol 4N+2 and Bits [7:0] in Symbol 4N+3 as it forwards the Control SKP Ordered Set in the Upstream direction if it is the target Receiver of a Margin Command and is executing the command.

• On receipt of a Control SKP Ordered Set, the Downstream Port must reflect the Margining Lane Status Register from the corresponding fields in the received Control SKP Ordered Set within 1 μs, if it passes the Margin CRC and Margin Parity checks and one of the following conditions apply:

•如果Retimer是余量命令的目标接收器并正在执行该命令，则在向上游方向转发控制SKP有序集时，Retimer必须覆盖符号4N+1的位[4:0]、符号4N+2的位[7,5:0]和符号4N+3的位[7:0]。

•在收到控制SKP有序集时，如果下游端口通过了余量CRC和余量奇偶校验，并且以下条件之一适用，则下游端口必须在1μs内从收到的控制SKP顺序集中的相应字段中反映链路余量测试状态寄存器：

◦ In the Margining Lane Control Register: Receiver Number is 010b through 101b

◦ In the Margining Lane Control Register: Receiver Number is 000b, Margin Command is Clear Error Log, No Command, or Go to Normal Settings, and there are Retimer(s) in the Link

◦ Optionally, if the Margining Lane Control Register Usage Model field is 1b

◦ Optionally, if the Margining Lane Control Register Receiver Number field is 110b or 111b

◦ 在链路余量测试控制寄存器中：接收器编号为010b到101b

◦ 在链路余量测试控制寄存器中：接收器编号为000b，余量命令为清除错误日志、无命令或转到正常设置，并且链路中有Retimer

◦ 可选地，如果链路余量测试控制寄存器使用模型字段为1b

◦ 可选地，如果链路余量测试控制寄存器接收器编号字段是110b或111b

The Margining Lane Status Register fields are updated regardless of the Usage Model bit in the received Control SKP Ordered Set.

• A component must advertise the same value for each parameter defined in Table 8-11 in Section 8.4.4 across all its Receivers. A component must not change any parameter value except for MSampleCount and MErrorCount defined in Table 8-11 in Section 8.4.4 while LinkUp = 1b.

不管接收到的控制SKP有序集合中的使用模型位如何，都会更新链路余量测试状态寄存器字段。

•组件必须在其所有接收器上公布第8.4.4节表8-11中定义的每个参数的相同值。当LinkUp=1b时，组件不得更改任何参数值，第8.4.4节表8-11中定义的MSampleCount和MErrorCount除外。

• A target Receiver that receives a valid Step Margin command must continue to apply that offset until any of the following occur:

◦ it receives a valid Go to Normal Settings command

◦ it receives a subsequent valid Step Margin command with different Margin Type or Margin Payload field

◦ MIndErrorSampler is 0b and MErrorCount exceeds Error Count Limit

◦ Optionally, MIndErrorSampler is 1b and MErrorCount exceeds Error Count Limit.

•接收到有效阶跃余量命令的目标接收器必须继续应用该偏移，直到出现以下任何情况：

◦ 它收到一个有效的“转到正常设置”命令

◦ 它接收到具有不同余量类型或余量有效载荷字段的后续有效阶跃余量命令

◦ MIndErrorSampler为0b，并且MErrorCount超过错误计数限制

◦ 可选地，MIndErrorSampler为1b，并且MErrorCount超过错误计数限制。

• If a Step Margin command terminates because MErrorCount exceeds Error Count Limit, the target Receiver must automatically return to its default sample position and indicate this in the Margin Payload field (Step Margin Execution Status = 00b). Note: termination for this reason is optional if MIndErrorSampler is 1b.

• If MIndErrorSampler is 0b, an error is detected when:

◦ The target Receiver is a Port that enters Recovery or detects a Data Parity mismatch while in L0

◦ The target Receiver is a Pseudo Port that enters Forwarding training sets or detects a Data Parity mismatch while forwarding non-training sets.

•如果由于错误计数超过错误计数限制而导致步进余量命令终止，则目标接收器必须自动返回到其默认样本位置，并在余量有效载荷字段中指出这一点（步进余量执行状态=00b）。注意：如果MIndErrorSampler为1b，则出于此原因终止是可选的。

•如果MIndErrorSampler为0b，则在以下情况下检测到错误：

◦ 目标接收器是在L0中进入恢复或检测到数据奇偶校验不匹配的端口

◦ 目标接收器是进入转发训练集或在转发非训练集时检测到数据奇偶校验不匹配的伪端口。

• If MIndErrorSampler is 1b, an error is detected when:

◦ The target Receiver is a Port and a bit error is detected while in L0

◦ The target Receiver is a Pseudo Port and a bit error is detected while the Retimer is forwarding non-training sets

•如果MIndErrorSampler为1b，则在以下情况下检测到错误：

◦ 目标接收器是一个端口，在L0中检测到一个位错误

◦ 目标接收器是伪端口，在Retimer转发非训练集时检测到比特错误

• If MIndErrorSampler is 0b and either (1) the target Receiver is a Port that enters Recovery or (2) the target Receiver is a Pseudo Port that enters Forwarding training sets:

◦ The target Receiver must go back to the default sample position

◦ If the target Receiver is a Port that is still performing margining, it must resume the margin position within 128 μs of entering L0

◦ If the target Receiver is a Pseudo Port that is still performing margining, it must resume the margin position within 128 μs of Forwarding non-training sets

•如果MIndErrorSampler为0b，并且（1）目标接收器是进入恢复的端口，或者（2）目标接收器为进入转发训练集的伪端口：

◦ 目标接收器必须返回到默认样本位置

◦ 如果目标接收器是仍在执行余量的端口，则必须在输入L0后128μs内恢复余量位置

◦ 如果目标接收器是仍在执行余量处理的伪端口，则它必须在转发非训练集的128μs内恢复余量位置

• A target Receiver is required to clear its accumulated error count on receiving Clear Error Log command, while it continues to margin (if it is the target Receiver of a Step Margin command still in progress), if it was doing so.

• For a target Receiver of a Set Error Count Limit command, the new value is used for all future Step Margin commands until a new Set Error Count Limit command is received.

• If no Set Error Count Limit is received by a Receiver since entering L0, the default value is 4.

• Behavior is undefined if a Set Error Count Limit command is received while a Step Margin command is in effect.

• Once a target Receiver reports a Step Margin Execution Status of 11b (NAK) or 00b ('Too many errors'), it must continue to report the same status as long as the Step Margin command is in effect.

•目标接收器需要在接收到清除错误日志命令时清除其累积错误计数，同时继续余量（如果它是仍在进行的步长余量命令的目标接收器），如果它正在这样做的话。

•对于Set Error Count Limit（设置错误计数限制）命令的目标接收器，新值将用于所有未来的阶跃余量命令，直到接收到新的Set Error Count Limited（设置错误数限制）命令。

•如果自输入L0后，接收器未收到设置错误计数限制，则默认值为4。

•如果在阶跃余量命令生效时收到“设置错误计数限制”命令，则行为未定义。

•一旦目标接收器报告阶跃余量执行状态为11b（NAK）或00b（“错误太多”），只要阶跃裕量命令有效，它就必须继续报告相同的状态。

• A target Receiver must not report a Step Margin Execution Status of 01b ('Set up for margin in progress') for more than 100 ms after it receives a new valid Step Margin command

• A target Receiver that reports a Step Margin Execution Status other than 01b, cannot report 01b subsequently unless it receives a new valid Step Margin command.

• Reserved bits in the Margin Payload must follow these rules:

◦ The Downstream or Upstream Port must transmit 0s for Reserved bits

◦ The retimer must forward Reserved bits unmodified

◦ All Receivers must ignore Reserved bits

•目标接收器在收到新的有效阶跃余量命令后的100毫秒内，不得报告01b的阶跃裕量执行状态（“正在设置余量”）

•报告01b以外的阶跃余量执行状态的目标接收器不能随后报告01b，除非它接收到新的有效阶跃裕量命令。

•余量有效载荷中的保留位必须遵循以下规则：

◦ 下行或上行端口必须传输0作为保留位

◦ 重定时器必须转发未修改的保留位

◦ 所有接收器必须忽略保留位

• Reserved encodings of the Margin Command, Receiver Number, or Margin Payload fields must follow these rules:

◦ The retimer must forward Reserved encodings unmodified

◦ All Receivers must treat Reserved encodings as if they are not the target of the Margin Command

• A Vendor Defined Margin Command or response, that is not defined by a retimer is ignored and forwarded normally.

• A target Receiver on a Retimer must return 00h on the response payload on Access Retimer register command, if it does not support register access. If a Retimer supports Access Retimer register command, the following must be observed:

◦ It must return a non-zero value for the DWORD at locations 80h and 84h respectively.

◦ It must not place any registers corresponding to Margin Payload locations 88h through 9Fh.

•余量命令、接收器编号或余量有效载荷字段的保留编码必须遵循以下规则：

◦ 重定时器必须转发未经修改的保留编码

◦ 所有接收器必须将保留编码视为它们不是余量命令的目标

•未由重定时器定义的供应商定义的余量命令或响应被忽略并正常转发。

•如果Retimer上的目标接收器不支持寄存器访问，则它必须在Access Retimer register命令的响应有效负载上返回00h。如果Retimer支持Access Retimer register命令，则必须遵守以下规定：

◦ 它必须分别在位置80h和84h为DWORD返回一个非零值。

◦ 它不得放置与裕量有效载荷位置88h到9Fh相对应的任何寄存器。

## 4.2.13.3 Receiver Margin Testing Requirements

Software must ensure that the following conditions are met before performing Lane Margining at Receiver:

• The current Link data rate must be 16.0 GT/s or higher.

• The current Link width must include the Lanes that are to be tested.

• The Upstream Port's Function(s) must be programmed to a D-state that prevents the Port from entering the L1 Link state. See Section 5.2 for more information.

• The ASPM Control field of the Link Control register must be set to 00b (Disabled) in both the Downstream Port and Upstream Port.

4.2.13.3接收机余量测试要求

在接收器处执行链路余量之前，软件必须确保满足以下条件：

•当前链路数据速率必须为16.0 GT/s或更高。

•当前链路宽度必须包括要测试的车道。

•上游端口的功能必须编程为D状态，以防止端口进入L1链路状态。有关更多信息，请参见第5.2节。

•在下行端口和上行端口中，链路控制寄存器的ASPM控制字段必须设置为00b（禁用）。

• The state of the Hardware Autonomous Speed Disable bit of the Link Control 2 register and the Hardware Autonomous Width Disable bit of the Link Control register must be saved to be restored later in this procedure.

• If writeable, the Hardware Autonomous Speed Disable bit of the Link Control 2 register must be Set in both the Downstream Port and Upstream Port. (If hardwired to 0b, the autonomous speed change mechanism is not implemented and is therefore inherently disabled.)

• If writeable, the Hardware Autonomous Width Disable bit of the Link Control register must be Set in both the Downstream Port and Upstream Port. (If hardwired to 0b, the autonomous width change mechanism is not implemented and is therefore inherently disabled.)

•必须保存链路控制2寄存器的硬件自主速度禁用位和链路控制寄存器的硬件自动宽度禁用位的状态，以便稍后在本过程中恢复。

•如果可写，则链路控制2寄存器的硬件自主速度禁用位必须在下行端口和上行端口中设置

•如果可写，则链路控制寄存器的硬件自主宽度禁用位必须在下行端口和上行端口中设置。（如果硬接线至0b，则未实现自主宽度更改机制，因此固有禁用。）

While margining, software must ensure the following:

• All Margin Commands must have the Usage Model field in the Margining Lane Control Register set to 0b. While checking for the status of an outstanding Margin Command, software must check that the Usage Model field of the status part of the Margining Lane Status Register is set to 0b.

• Software must read the capabilities offered by a Receiver and margin it within the constraints of the capabilities it offers. The commands issued and the process followed to determine the margin must be consistent with the definitions provided in Section 4.2.13 and Section 8.4.4 . For example, if the Port does not support voltage testing, then software must not initiate a voltage test. In addition, if a Port supports testing of 2 Lanes simultaneously, then software must test only 1 or 2 Lanes at the same time and not more than 2 Lanes.

在余量时，软件必须确保以下内容：

•所有余量指令必须将链路余量测试控制寄存器中的使用模型字段设置为0b。在检查未完成的余量命令的状态时，软件必须检查链路余量测试状态寄存器的状态部分的使用模型字段是否设置为0b。

•软件必须读取接收器提供的功能，并在其提供的功能的限制范围内进行余量。发出的命令和确定余量所遵循的过程必须与第4.2.13节和第8.4.4节中提供的定义一致。例如，如果端口不支持电压测试，则软件不得启动电压测试。此外，如果一个端口支持同时测试2条车道，则软件必须同时只测试1条或2条车道且不超过2条车道。

• For Receivers where MIndErrorSampler is 1b, any combination of such Receivers are permitted to be margined in parallel.

• For Receivers where MIndErrorSampler is 0b, at most one such Receiver is permitted to be margined at a time. However, margining may be performed on multiple Lanes simultaneously, as long as it is within the maximum number of Lanes the device supports.

• Software must ensure that the Margin Command it provides in the Margining Lane Control Register is a valid one, as defined in Section 4.2.13.1 . For example, the Margin Type must have a defined encoding and the Receiver Number and Margin Payload consistent with it.

•对于MIndErrorSampler为1b的接收器，允许对此类接收器的任何组合进行并行余量。

•对于MIndErrorSampler为0b的接收器，一次最多允许有一个这样的接收器。但是，只要在设备支持的最大车道数以内，就可以同时在多个车道上执行余量。

•软件必须确保其在链路余量测试控制寄存器中提供的余量命令是有效的，如第4.2.13.1节所定义。例如，余量类型必须具有定义的编码，并且接收器编号和余量有效载荷与其一致。

• After issuing a command by writing to the Margining Lane Control Register atomically, software must check for the completion of this command. This is done by atomically reading the Margining Lane Status Register and checking that the status fields match the expected response for the issued command (see Table 4-25 ). If 10 ms has elapsed after a new Margin Command was issued and the values read do not match the expected response, software is permitted to assume that the Receiver will not respond, and declare that the target Receiver failed margining. For a broadcast command other than No Command the Receiver Number in the response must correspond to one of the Pseudo Ports in Retimer Y or Retimer Z, as described in Figure 4-35 .

•通过原子写入链路余量测试控制寄存器发出命令后，软件必须检查该命令的完成情况。这是通过原子读取链路余量测试状态寄存器并检查状态字段是否与发出命令的预期响应匹配来完成的（见表4-25）。如果在发出新的余量命令后已经过了10毫秒，并且读取的值与预期响应不匹配，则允许软件假设接收器不会响应，并声明目标接收器未通过余量。对于非“无命令”的广播命令，响应中的接收器编号必须对应于Retimer Y或Retimer Z中的伪端口之一，如图4-35所示。

• Any two reads of the Margining Lane Status Register should be spaced at least 10 μs apart to make sure they are reading results from different Control SKP Ordered Sets.

• Software must broadcast No Command and wait for it to complete prior to issuing a new Margin Type or Receiver Number or Margin Payload in the Margining Lane Control Register.

• At the end of margining in a given direction (voltage/ timing and up/down/left/right), software must broadcast Go to Normal Settings, No Command, Clear Error Log, and No Command in series in the Downstream and Upstream Ports, after ensuring each command has been acknowledged by the target Receiver.

•链路余量测试状态寄存器的任何两次读取应间隔至少10μs，以确保它们是从不同的控制SKP有序集读取结果。

•在链路余量测试控制寄存器中发布新的余量类型或接收器编号或余量有效载荷之前，软件必须广播“无命令”并等待其完成。

•在给定方向（电压/定时和上/下/左/右）的余量结束时，软件必须在确保每个命令都已被目标接收器确认后，在下游和上游端口中串行广播“转到正常设置”、“无命令”、“清除错误日志”和“无命令。

• If the Data Rate has changed during margining, margining results (if any) are not accurate and software must exit the margining procedure. Software must set the Margining Lane Control Register to No Command to avoid starting margining if the Data Rate later changes to 16.0 GT/s or higher.

• Software is permitted to issue a Clear Error Log command periodically while margining is in progress, to gather error information over a long period of time.

• Software must not attempt to margin both timing and voltage of a target Receiver simultaneously. Results are undefined if a Receiver receives commands that would place both voltage and timing margin locations away from the default sample position at the same time.

•如果数据速率在余量计算过程中发生变化，余量计算结果（如有）不准确，软件必须退出余量计算程序。如果数据速率后来更改为16.0 GT/s或更高，软件必须将余量车道控制寄存器设置为无命令，以避免开始余量。

•允许软件在余量处理过程中定期发出“清除错误日志”命令，以在很长一段时间内收集错误信息。

•软件不得试图同时余量目标接收器的定时和电压。如果接收器接收到将电压和定时余量位置同时放置在远离默认采样位置的命令，则结果是未定义的。

• Software should allow margining to run for at least 108 bits margined by the Receiver under test before switching to the next margin step location (unless the error limit is exceeded).

• Software must account for the 'set up for margin in progress' status while measuring the margin time or the number of bits sampled by the Receiver.

• If a target Receiver is reporting 'set up for margin in progress' for 200 ms after issuing one of the Step Margin commands, Software is permitted to assume that the Receiver will not respond and declare that the target Receiver failed margining.

•在切换到下一个余量步长位置之前，软件应允许余量运行至少108位，由受测接收器余量（除非超过误差限制）。

•在测量余量时间或接收器采样的位数时，软件必须考虑到“正在设置余量”状态。

•如果目标接收器在发出其中一个阶跃余量命令后200毫秒内报告“正在进行余量设置”，则允许软件假设接收器不会做出响应，并声明目标接收器未通过余量设置。

• If a Receiver reports a 'NAK' in the Margin Payload status field and the corresponding Step Margin command was valid and within the allowable range (as defined in Section 4.2.13 and Section 8.4.4 ), Software is permitted to declare that the target Receiver failed margining.

• When the margin testing procedure is completed, the state of the Hardware Autonomous Speed Disable bit and the Hardware Autonomous Width Disable bit must be restored to the previously saved values.

•如果接收器在余量有效载荷状态字段中报告“NAK”，并且相应的阶跃余量命令有效且在允许范围内（如第4.2.13节和第8.4.4节所定义），则允许软件声明目标接收器未通过余量。

•当余量测试程序完成时，硬件自主速度禁用位和硬件自主宽度禁用位的状态必须恢复到以前保存的值。

**IMPLEMENTATION NOTE**

Example Software Flow for Lane Margining at Receiver

For getting the invariant parameters the following steps may be followed. Once obtained, the same parameters can be used across multiple sets of margining tests as long as LinkUp=1b continues to be true. For each component in the Link, do the following Steps. Software can do these steps in parallel for different components on different Lanes of the Link.

实施说明

接收器处链路余量的示例软件流程

为了获得不变参数，可以遵循以下步骤。一旦获得，只要LinkUp=1b继续为真，就可以在多组边际测试中使用相同的参数。对于链接中的每个组件，请执行以下步骤。软件可以对链路的不同车道上的不同组件并行执行这些步骤。

***Step A1*:**

Issue Report Margin Control Capabilities (Margin Type = 001b, Margin Payload = 88h, Receiver Number = target device in the Margining Lane Control Register)

步骤A1：

发布报告余量控制能力（余量类型=001b，余量有效载荷=88h，接收器编号=余量车道控制寄存器中的目标设备）

***Step A2*:**

Read the Margining Lane Status Register.

a. If Margin Type = 001b and Receiver Number = target Receiver: Go to Step A3

b. Else: If 10 ms has expired since command issued, declare Receiver failed margining and exit; else wait for >10 μs and Go to Step A2

***Step A3*:**

Store the information provided Margin Payload status field for use during margining.

步骤A2：

读取链路余量测试状态寄存器。

a.如果余量类型=001b且接收器编号=目标接收器：转至步骤A3

b.否则：如果自发出命令以来已超过10毫秒，则声明Receiver失败余量并退出；否则等待>10μs，然后转到步骤A2

步骤A3：

存储提供的余量有效载荷状态字段的信息，以便在余量期间使用。

***Step A4*:**

Broadcast No Command (Margin Type = 111b, Receiver Number = 000b, and Margin Payload = 9Ch in the Margining Lane Control Register) and wait for those to be reflected back in the Margining Lane Status Register. If 10 ms expires without getting the command completion handshake, declare the Receiver failed margining and exit.

步骤A4：

广播无命令（链路余量测试控制寄存器中的余量类型=111b、接收器编号=000b和余量有效载荷=9Ch），并等待这些命令反映回链路余量测试状态寄存器。如果10毫秒到期而没有获得命令完成握手，则声明Receiver failed margining并退出。

***Step A5*:**

Repeat Step A1 through Step A4 for Report MNumVoltageSteps, Report MNumTimingSteps, Report MMaxTimingOffset, Report MMaxVoltageOffset, Report MSamplingRateVoltage, and Report MSamplingRateTiming. It may be noted that this step can be executed in parallel across different Lanes for different Margin Type.

Margining on each Lane across the Link can be a sequence of separate commands. Prior to launching the sequence, software should read the maximum number of Lanes it is allowed to run margining simultaneously.

步骤A5：

对于Report MNumVoltageSteps、Report MNumTimingSteps、Reporting MMaxTimingOffset、Report MMaxVoltageOffset、ReportMSamplingRateVoltage和Report MSamplingRateTiming，重复步骤A1至步骤A4。可以注意到，对于不同的余量类型，该步骤可以在不同车道上并行执行。

链路上每条车道上的余量可以是一系列单独的命令。在启动序列之前，软件应读取允许同时运行余量的最大车道数。

The steps would be similar to Step A1 through Step A4 above with the Report MMaxLanes command. After that software can simultaneously margin up to that many Lanes of the Link. On each Link, each Receiver is margined based on its capability, subject to the constraints described here, after ensuring the Link is operating at full width in 16.0 GT/s or higher Data Rate and the hardware autonomous width and speed change as well as ASPM power states have been disabled.

If software desires to set an Error Count Limit value different than default of 4 or whatever was programmed last, it executes the following Steps prior to going to Step C1 below.

这些步骤将类似于上面使用Report MMaxLanes命令的步骤A1到步骤A4。在那之后，软件可以同时为链接的许多车道留出余量。在每个链路上，在确保链路以16.0 GT/s或更高的数据速率以全宽运行，并且硬件自主宽度和速度变化以及ASPM功率状态已被禁用后，根据其能力，根据此处描述的约束条件，对每个接收器进行裕量处理。

如果软件希望设置一个不同于默认值4的错误计数极限值或上次编程的任何值，则在进入下面的步骤C1之前，执行以下步骤。

***Step B1*:**

Issue Set Error Count Limit (Margin Type = 010b, the target Receiver Number, and Margin Payload = {11b, Error Count Limit} in the Margining Lane Control Register)

***Step B2*:**

Read the Margining Lane Status Register.

a. If Margin Type = 010b, Receiver Number = target Receiver, and Margin Payload = Margin Payload control field (Bits [14:7]), go to Step B4

b. Else: If 10 ms has expired since command issued, go to Step B3; else wait for >10 μs and Go to Step B2

步骤B1：

问题设置错误计数限制（余量类型=010b，目标接收器编号，余量有效载荷=｛11b，链路余量测试控制寄存器中的错误计数限制｝）

步骤B2：

读取链路余量测试状态寄存器。

a.如果裕量类型=010b，接收器编号=目标接收器，且裕量有效载荷=裕量有效负载控制字段（位[14:7]），则转至步骤B4

b.否则：如果自发出命令以来已经超过10ms，则转到步骤B3；否则等待>10μs，然后转到步骤B2

***Step B3*:**

Margining has failed. Invoke the system checks to find out if the Link degraded in width/speed due to reliability reasons.

***Step B4*:**

Broadcast No Command and wait for those to be reflected back in the status fields. If 10 ms expires without getting the command completion handshake, declare the Receiver failed margining and exit. The following steps is an example flow of one margin point for a given Receiver executing Step Margin to timing offset to right/left of default starting with 15 steps to the right:

步骤B3：

余量已失败。调用系统检查以查明链路的宽度/速度是否由于可靠性原因而降低。

步骤B4：

广播无命令，并等待这些命令在状态字段中反映出来。如果10毫秒到期而没有获得命令完成握手，则声明Receiver failed margining并退出。以下步骤是给定接收器的一个余量点的示例流程，该接收器执行从向右15步开始的默认向右/向左定时偏移的步骤余量：

***Step C1*:**

Write Margin Type = 011b, the target Receiver Number, and Margin Payload = {0000b, 1111b} in the Margining Lane Control Register

***Step C2*:**

Read the Margining Lane Status Register.

a. If Margin Type = 011b and Receiver Number = target Receiver, Go to Step C3

b. Else If 10 ms has expired since command issued, declare Receiver has failed margining and go to Step C7

c. Wait for >10 μs and Go to Step C2

步骤C1：

在链路余量测试控制寄存器中写入余量类型=011b、目标接收器编号和余量有效载荷=｛0000b，1111b｝

步骤C2：

读取链路余量测试状态寄存器。

a.如果余量类型=011b且接收器编号=目标接收器，则转至步骤C3

b.否则，如果自发出命令以来10 ms已过期，则声明Receiver未通过余量，并转至步骤C7

c.等待>10μs，然后转到步骤C2

***Step C3*:**

In the Margining Lane Status Register:

a. If Margin Payload [7:6] = 11b:

i. If we exceeded the 0.2 UI, that is the margin;

ii. Else report margin failure at this point and go to Step C7;

b. Else if Margin Payload [7:6] = 00b:

i. report margin failure at this point and go to Step C7

步骤C3：

在链路余量测试状态寄存器中：

a.如果裕量有效载荷[7:6]=11b：

i.如果我们超过了0.2 UI，那就是差额；

ii。否则，报告此时的余量故障，并转到步骤C7；

b.否则，如果裕量有效载荷[7:6]=00b：

i.报告此时的余量故障，并转至步骤C7

c. Else if Margin Payload [7:6] = 01b:

i. If 200 ms has elapsed since entering Step C3, report that the Receiver failed margining test and exit;

ii. else wait 1 ms, read the Margining Lane Status Register and go to Step C3

d. Else go to Step C4

c.否则，如果裕量有效载荷[7:6]=01b：

i.如果自进入步骤C3以来已经过去了200ms，则报告接收器未通过裕量测试并退出；

ii。否则等待1毫秒，读取链路余量测试状态寄存器并进入步骤C3

d.否则，转至步骤C4

***Step C4*:**

Wait for the desired amount of time for margining to happen while sampling the Margining Lane Status Register periodically for the number of errors reported in the Margin Payload field (Bits [5:0] - MErrorCount).

For longer runs, issue the No Command follwed by the Clear Error Log commands, (using procedures similar to Step B1 through Step B4, with the corresponding expected status field) if the length of time will cause the error count to exceed the Set Error Count Limit even when staying within the expected BER target.

If the aggregate error count remains within the expected error count and the Margin Payload [7:6] in the status field remains 10b till the end, the Receiver has the required Margin at the timing margin step; else it fails that timing margin step go to Step C7.

步骤C4：

在对链路余量测试状态寄存器进行周期性采样以获取余量有效载荷字段中报告的错误数量（Bits[5:0]-MErrorCount）的同时，等待发生余量的所需时间。

对于较长的运行，如果时间长度将导致错误计数超过设置错误计数限制（即使在预期BER目标内），则发出“无命令”，然后发出“清除错误日志”命令（使用类似于步骤B1至步骤B4的过程，并带有相应的预期状态字段）。

如果总错误计数保持在预期错误计数内，并且状态字段中的余量有效载荷[7:6]保持10b直到结束，则接收机在定时余量步骤处具有所需余量；否则该定时余量步骤失败，则进入步骤C7。

***Step C5*:**

Broadcast No Command and wait for those to be reflected back in the status fields. If 10 ms expires without getting the command completion handshake, declare the Receiver failed margining and exit.

***Step C6*:**

Go to Step C1, incrementing the number of timing steps through the Margin Payload control field (Bits[5:0]) if we want to test against a higher margin amount; else go to Step C8 noting the margin value that the Receiver passed

步骤C5：

广播无命令，并等待这些命令在状态字段中反映出来。如果10毫秒到期而没有获得命令完成握手，则声明Receiver failed margining并退出。

步骤C6：

转到步骤C1，如果我们想要针对更高的裕量进行测试，则通过裕量有效载荷控制字段（Bits[5:0]）增加定时步数；否则进入步骤C8，注意接收器通过的余量值

***Step C7*:**

Margin failed; The previous margin step the Receiver passed in Step C6 is the margin of the Receiver

***Step C8*:**

Broadcast No Command, Clear Error Log, No Command, Go to Normal Settings series of commands (using a procedure similar to Step B1 through Step B4 with the corresponding expected status fields)

步骤C7：

余量失败；接收器在步骤C6中通过的先前余量步骤是接收器的余量

步骤C8：

广播无命令、清除错误日志、无命令、转到正常设置一系列命令（使用类似于步骤B1至步骤B4的程序以及相应的预期状态字段）

# 8.4.4 Lane Margining at the Receiver - Electrical Requirements

PCI Express components including retimers that support the 16.0 GT/s rate are required to support Lane margining at the Receiver when operating at 16.0 or 32.0 GT/s. Lane Margining enables system software to get the margin information of a given Lane while the Link is in L0 state. The margin information includes both voltage and time, in either direction from the current Receiver position. The margin feature is not permitted to require any additional external hardware to function. Support of Lane margining for voltage is optional at 16.0 GT/s and required at 32.0 GT/s and support of independent timing margin to the left or to the right is optional. For simplicity, the margin commands and requirements described in the protocol chapter(s) of this specification are described in terms of moving the data sample location – but the actual margining method is implementation specific. For example - the timing margin could be implemented on the actual data sampler or an independent/error sampler. Further the timing margin can be achieved by injecting an appropriate amount of stress/jitter to the data sample location, or by actually moving the data/error sample location.

The parameters in Table 8-11 are reported for 16.0 and 32.0 GT/s and are allowed to be different for each speed.

当以16.0或32.0 GT/s运行时，需要PCI Express组件（包括支持16.0 GT/s速率的重定时器）来支持接收器的链路裕量。链路裕量使系统软件能够在链路处于L0状态时获取给定链路的裕量信息。裕度信息包括从当前接收器位置向任一方向的电压和时间。边缘功能不允许需要任何额外的外部硬件来运行。在16.0 GT/s时，支持电压链路裕度是可选的，在32.0 GT/s时是必需的，支持向左或向右的独立定时裕度也是可选的。为简单起见，本规范协议章节中描述的裕量命令和要求是根据移动数据样本位置来描述的，但实际的裕量方法是特定于实现的。例如，定时裕度可以在实际数据采样器或独立/误差采样器上实现。此外，可以通过向数据采样位置注入适量的应力/抖动，或者通过实际移动数据/误差采样位置来实现定时裕度。

表8-11中的参数报告为16.0和32.0 GT/s，允许每种速度不同。

